US-PAT-NO: 6709874

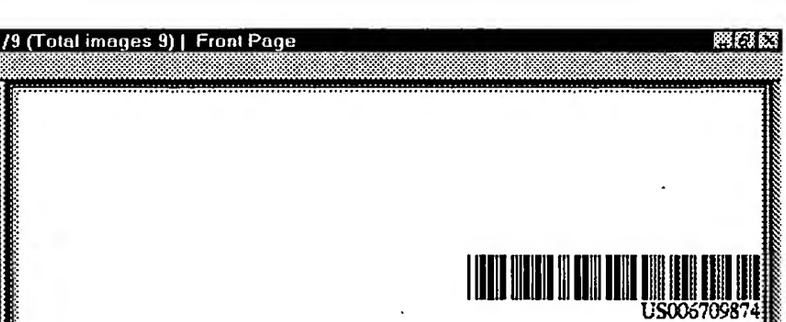
DOCUMENT-IDENTIFIER: US 6709874 B2
See image for Certificate of Correction

TITLE: Method of manufacturing a metal cap layer for preventing damascene conductive lines from oxidation

---------- KWIC ---------

Brief Summary Text - BSTX (7):
A disadvantage of manufacturing MRAMs is that copper is the preferred material for conductive lines, due to the excellent conductive properties of copper compared to aluminum and other conventional metals used in semiconductor technology. A problem with using copper in the BEOL is that the copper-conductive lines must be formed using a damascene process. In a damascene process, a dielectric layer is formed, and the dielectric layer is patterned and etched to form trenches that the conductive copper lines will be formed in. When copper is used, typically a seed layer and other copper liners are used, followed by a copper fill that may be electroplated for improved fill results, for example. Copper is unable to be etched directly due to the process limitations of the copper material.

Detailed Description Text - DETX (4):
In copper damascene BEOL prior art structures, to form copper wiring patterns, copper is deposited over patterns or trenches in an inter-level-dielectric (ILD) and then chemically-mechanically polished (CMP). A dielectric cap layer comprised of silicon nitride, for example, is usually deposited over the copper to protect the exposed copper surface, because copper is easily oxidized. This silicon nitride cap layer is etched using a hard mask during the next level via RIE process to protect the copper from exposing to the resist striping process.



(12) **United States Patent**
Ning

(10) **Patent No.: US**
(45) **Date of Patent:**

(54) **METHOD OF MANUFACTURING A METAL CAP LAYER FOR PREVENTING DAMASCENE CONDUCTIVE LINES FROM OXIDATION**

(75) Inventor: **Xian J. Ning**, Mohegan Lake, NY (US)

(73) Assignee: **Infineon Technologies AG**, Munich (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 18 days.

(21) Appl. No.: 09/798,101

(22) Filed: Mar. 2, 2001

(65) **Prior Publication Data**

US 2002/0096775 A1 Jul. 25, 2002

Related U.S. Application Data

(60) Provisional application No. 60/263,993, filed on Jan. 24, 2001.

(51) **Int. Cl.**[7] **H01L 21/00**

(52) **U.S. Cl.** 438/3; 438/625; 438/626; 438/627; 438/628; 438/629; 438/631; 438/642; 438/643; 438/644; 438/645; 438/648; 438/652; 438/653; 438/654; 438/656; 438/669; 438/672; 438/685; 438/687; 438/688; 438/622

(58) **Field of Search** 438/3, 522, 625–629, 438/631, 642–645, 648, 652–654, 656, 669, 672, 685, 687, 688

(56) **References Cited**

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Maria Peterson, et al., Controlling scene Structures Through Slurry I VMIC Conference, 1999 IMIC.

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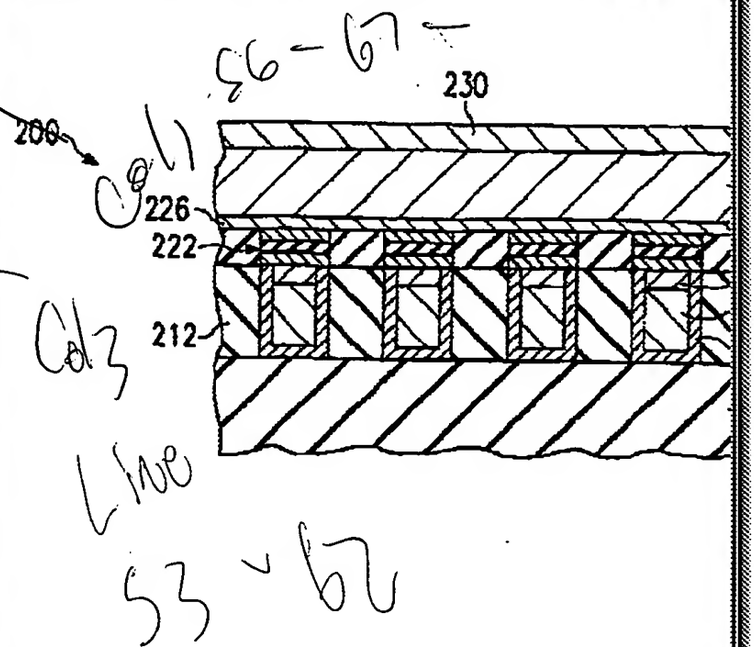
Primary Examiner—Evan Pert
Assistant Examiner—David A. Zar
(74) *Attorney, Agent, or Firm*—Sla

(57) **ABSTRAC**

A semiconductor device (100) havi BEOL structure. A metal cap laye conductive lines (118) to prevent ox lines (118) during subsequent proc cap layer (120) comprises a materia tive line (118) material that is res structure (100) is particularly benefi

20 Claims, 1 Drawi



6,635,490
6,440,753

US 20020098676A1

(19) **United States**

(12) **Patent Application Publication** (10) Pub. No.: US 2002

Ning et al. (43) Pub. Date:

(54) **METAL HARD MASK FOR ILD RIE PROCESSING OF SEMICONDUCTOR MEMORY DEVICES TO PREVENT OXIDATION OF CONDUCTIVE LINES**

(76) Inventors: Xian J. Ning, Mohegan Lake, NY (US); Joachim Nuetzel, Fishkill, NY (US)

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(21) Appl. No.: 09/824,596

(22) Filed: Apr. 2, 2001

Related U.S. Applicatio

(63) Non-provisional of provisio 60/263,991, filed on Jan. 24, 2

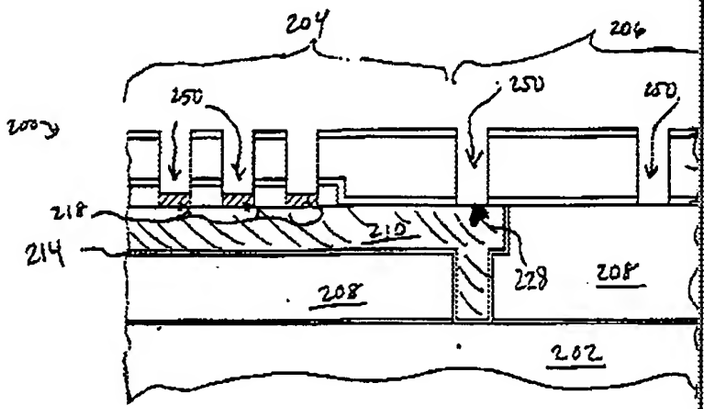
Publication Classific

(51) Int. Cl.[7] .....

(52) U.S. Cl. .....

(57) **ABSTRACT**

memory array integrated circuit (200 (244) and reactive ion etching (RIE) (244) prevents oxidation of underly (210).



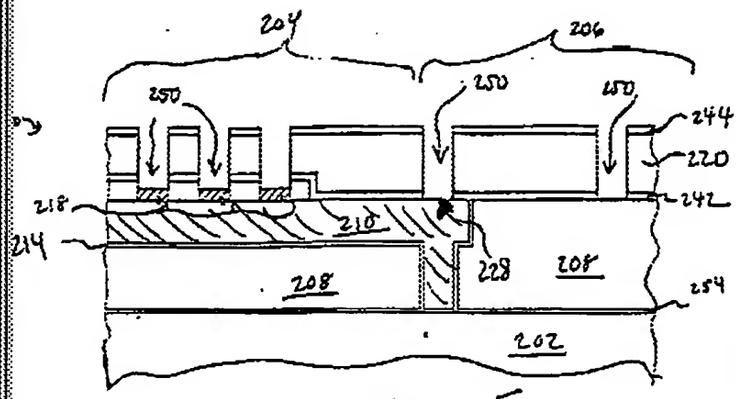


Fig. 5

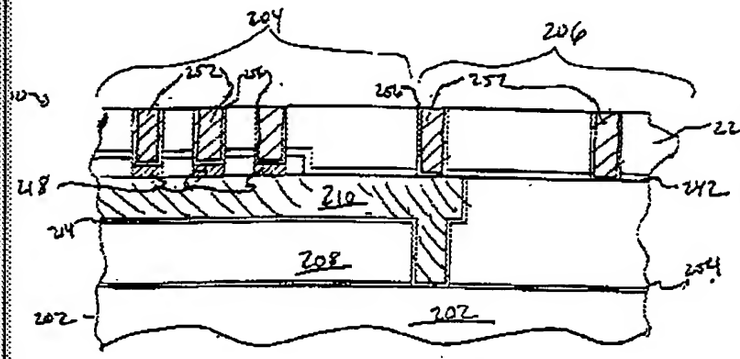


Fig. 6

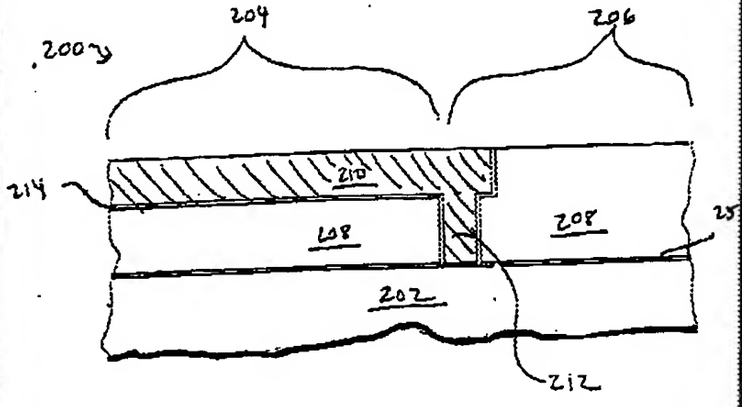


Fig. 1

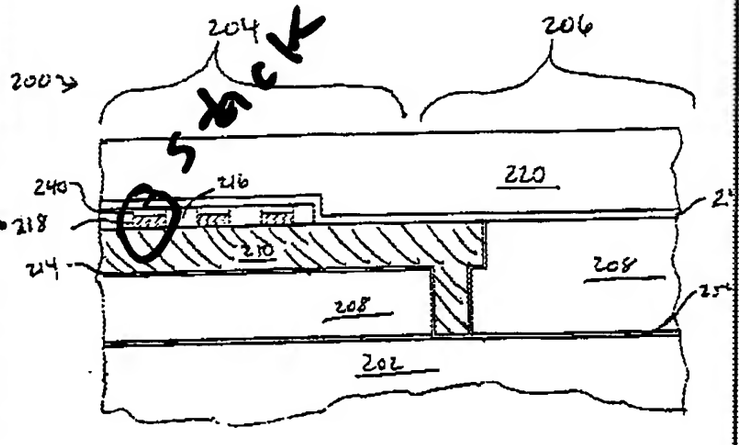


Fig. 2

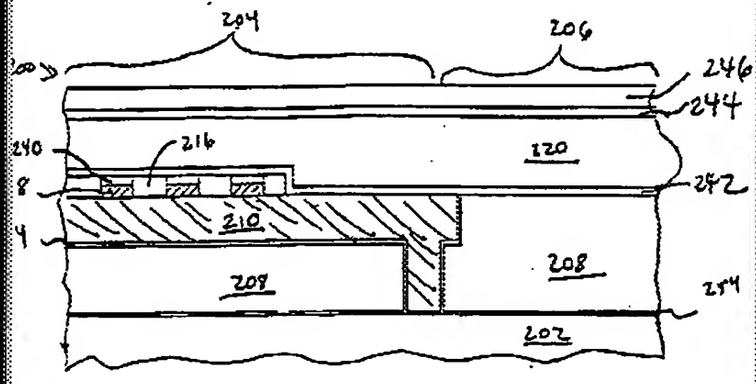


Fig. 3

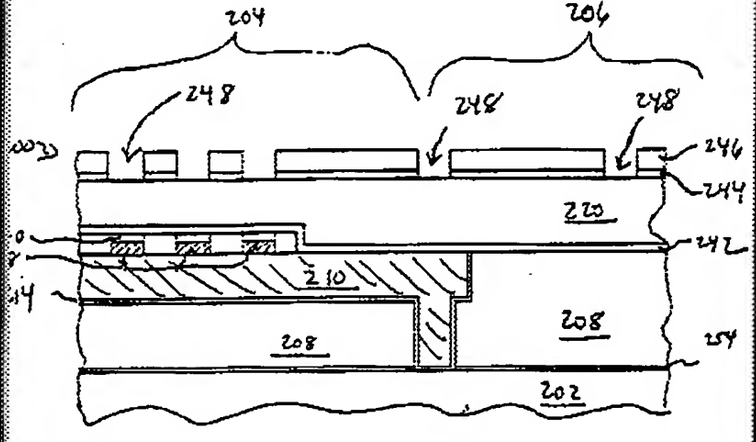


Fig 4

substrate 202 with a first ILD layer 208 deposited thereon is provided. The substrate 200 comprises array and non-array regions 204 and 206, respectively. The ILD layer 208 may be adjacent first conductive lines 210 and vias 212 that connect the first conductive lines 210 to underlying circuit elements (not shown), for example. Other components that are not shown may be included in the substrate non-array region 206. The first ILD layer 208 preferably comprises a dielectric such as silicon dioxide, for example. ILD layer 208 may alternatively comprise other types of suitable dielectric materials, such as Silk.TM., fluorinated silicon glass, FOX.TM., as examples.

[0025] A plurality of first conductive lines 210 are formed within the first ILD layer 208 using a damascene process, for example. Preferably, first conductive lines 210 in the array region 204 run in a first direction and serve as bitlines or wordlines of the memory array in the array region 204. Typically, the first conductive lines 210 are located on a first or second metal level (M1 or M2 level) of the IC 200.

[0026] Referring to FIG. 2, memory cell material 218 is deposited over dielectric layer 208 and conductive lines 210. In one embodiment, the memory cell material 218 comprises magnetic stack material in the array region 204. The magnetic stack material 218 may comprise, for example, a plurality of layers comprising PtMn, CoFe, Ru, Al.sub.2O.sub.3, NiFe, although other types of suitable magnetic materials may be used sandwiched around an insulating layer. The magnetic stacks 218 preferably comprise a bottom layer comprising several layers of magnetic materials, an insulating layer comprising Al.sub.2O.sub.3 for example, the insulating layer providing a tunnel junction (TJ). A top layer comprising several layers of magnetic materials is formed over the insulating layer. Various techniques, such as physical vapor deposition (PVD), evaporation, and chemical vapor deposition (CVD) may be used to deposit the various magnetic and insulating layers. Because each layer of

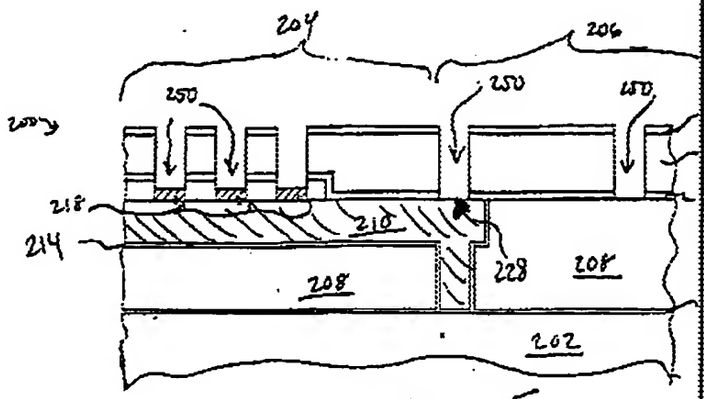


Fig. 5

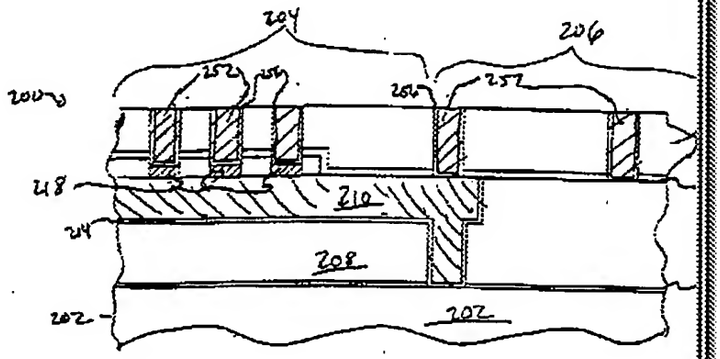


Fig. 6

tunnel

insulating layers. Because each layer of magnetic material is very thin, e.g., less than 100 Angstroms, the magnetic material deposition preferably is by PVD, although other methods may be used. The magnetic stack 218 bottom magnetic layer is coupled to and makes electrical contact with the conductive lines 210 which may comprise wordlines, for example.

[0027] In accordance with the present invention, a layer 240 is deposited over the magnetic stacks 218. The layer 240 serves as hard mask for the magnetic stack 218 etch. The hard mask layer 240 may comprise, for example, an oxide cap comprising silicon oxide. Alternatively, the hard mask layer 240 may comprise other materials such as TiN, W, TaN, Ta, as examples. The hard mask layer 240 and magnetic layers are then patterned to form magnetic stacks 218. A resist (not shown) may be deposited and patterned with the magnetic stack pattern, and the pattern transferred to the hard mask layer 240. The resist is removed and the hard mask layer 240 is used to pattern the magnetic stack material 218.

[0028] Next, a dielectric layer 216, such as silicon nitride, is deposited over the magnetic stacks 218, filling the spaces between the magnetic stacks 218. The wafer 200 is planarized by, for example, chemical-mechanical polishing (CMP) using the hard mask layer or oxide cap 240 as a polish stop. The CMP process removes excess silicon nitride 216 to provide a planar surface which is co-planar with the silicon oxide cap 240.

[0029] A photo-lithography and etch process (not shown) are used to remove layer 216 in non-array region 206. Then a dielectric liner 242 is deposited over the magnetic stacks 218, conductive lines 210, and dielectric 208. The dielectric liner 242 preferably comprises silicon nitride and alternatively may comprise silicon carbide, for example. The dielectric liner 242 may be, for example, about 300 Angstroms thick. The dielectric liner 242 serves as an etch stop layer for subsequent processing steps.

[0030] A dielectric layer 220 is deposited over the dielectric liner 242, as shown in FIG. 2. The dielectric layer 220 serves as an ILD layer. The dielectric layer 220 preferably comprises, for example, silicon oxide. Alternatively, dielectric layer 220 may comprise other dielectric materials such as Silk.TM., fluorinated silicon glass, FOX.TM., as examples. The surface of the dielectric layer 220 is planarized, for example, by CMP to provide a

US 20020098676A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 200**

Ning et al. (43) **Pub. Date:**

(54) **METAL HARD MASK FOR ILD RIE PROCESSING OF SEMICONDUCTOR MEMORY DEVICES TO PREVENT OXIDATION OF CONDUCTIVE LINES**

(76) Inventors: **Xian J. Ning, Mohegan Lake, NY (US); Joachim Nuetzel, Fishkill, NY (US)**

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DALLAS, TX 75252-5793 (US)

(21) Appl. No.: **09/824,596**

(22) Filed: **Apr. 2, 2001**

Related U.S. Applicatio

(63) Non-provisional of provisio 60/263,991, filed on Jan. 24, 2

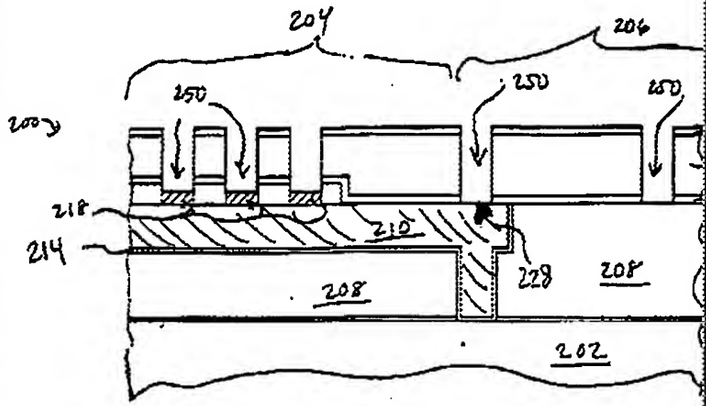
Publication Classific

(51) **Int. Cl.**[7] .....

(52) **U.S. Cl.** .....

(57) **ABSTRACT**

memory array integrated circuit (200 (244) and reactive ion etching (RIE) (244) prevents oxidation of underly (210).



US 20030234449A1

(19) **United States**

(12) **Patent Application Publication** (10) Pub. No.: US 2003/0234449 A1

Aratani et al. (43) Pub. Date: Dec. 25, 2003

(54) MEMORY DEVICE AND METHOD OF PRODUCTION AND METHOD OF USE OF SAME AND SEMICONDUCTOR DEVICE AND METHOD OF PRODUCTION OF SAME

(76) Inventors: Katsuhisa Aratani, Chiba (JP); Minoru Ishida, Tokyo (JP); Akira Kouchiyama, Kanagawa (JP)

Correspondence Address:
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(21) Appl. No.: 10/410,789

(22) Filed: Apr. 10, 2003

(30) Foreign Application Priority Data

Apr. 18, 2002 (JP) JP2002-116552
Aug. 22, 2002 (JP) JP2002-242653

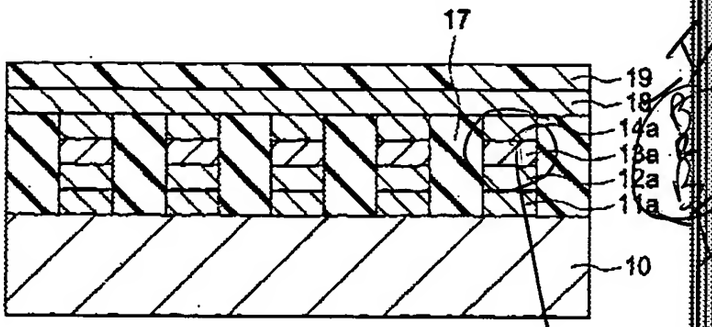
Publication Classification

(51) Int. Cl.[7] H01L 23/48

(52) U.S. Cl. 257/758

(57) ABSTRACT

A memory device able to be produced without requiring high precision alignment, a method of production of the same, and a method of use of a memory device produced in this way, wherein a peripheral circuit portion (first semiconductor portion) formed by a first minimum processing dimension is formed on a substrate, a memory portion (second semiconductor portion) formed by a second minimum processing dimension smaller than the first minimum processing dimension is stacked above it, and the memory portion (second semiconductor portion) is stacked with respect to the peripheral circuit portion (first semiconductor portion) with an alignment precision rougher than the second minimum processing dimension or wherein memory cells configured by 2-terminal devices are formed in regions where word lines and bit lines intersect in the memory portion, and contact portions connecting the word lines and bit lines and the peripheral circuit portions are arranged in at least two columns in directions in which the word lines and the bit lines extend.



MRAM

memory device

Fig 2

DOCUMENT-IDENTIFIER: US 20030234449 A1

TITLE: Memory device and method of production and method of use of same and semiconductor device and method of production of same

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Application Filing Date - APD (1):
20030410

Current US Classification, US Primary Class/Subclass - CCPR (1):
257/758

Summary of Invention Paragraph - BSTX (5):
[0004] As memory devices, mask read only memories (ROMs), programmable read only memories (PROMs), static random access memories (SRAMs), dynamic random accessor memories (DRAM), flash memories, ferroelectric random access memories (FeRAMs), magnetic random access memories (MRAM), phase change memories, and numerous other solid state memory devices have been developed and produced.

Detail Description Paragraph - DETX (112):
[0219] The inspection can be carried out by recording and reproduction in addition to electrical conduction. After the inspection, the address information or array information of the valid memory cells is stored in a memory provided in the peripheral circuits of a memory common circuit. As the memory used here, use can be made of a memory comprised of 2-terminal devices according to the present embodiment or a conventionally used SRAM, DRAM, flash memory, MRAM, FeRAM, fuse type or anti-fuse type memory, or other memory.

FIG. 3

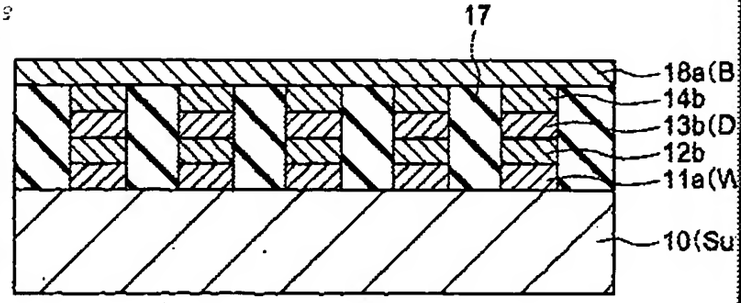


FIG. 4A

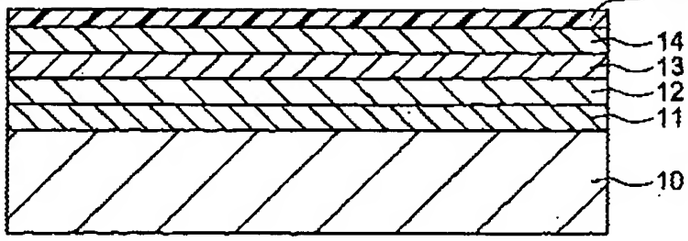


FIG. 4B

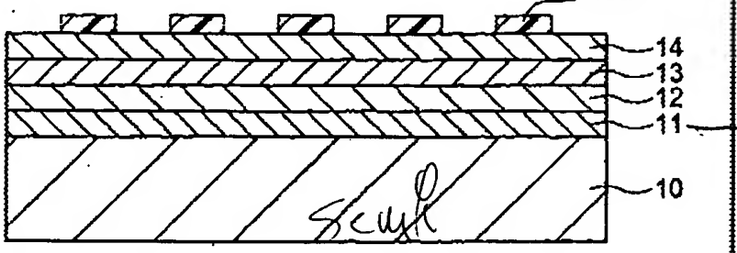


FIG. 5A

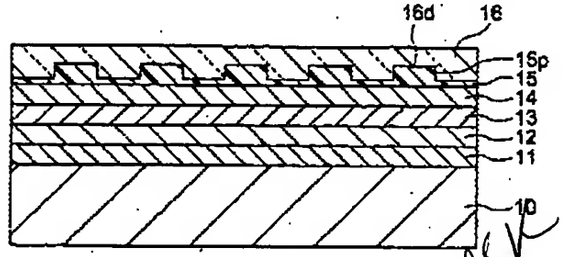


FIG. 5B

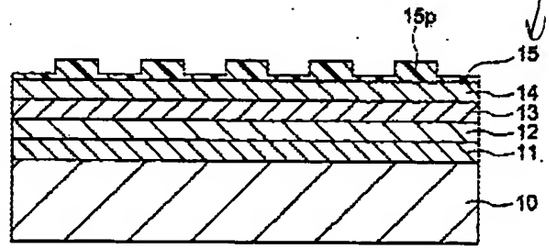


FIG. 6A

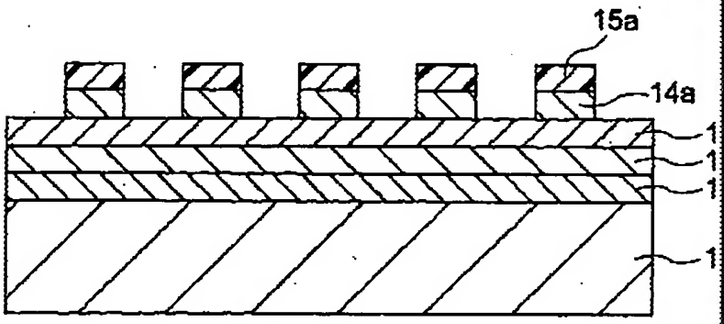


FIG. 6B

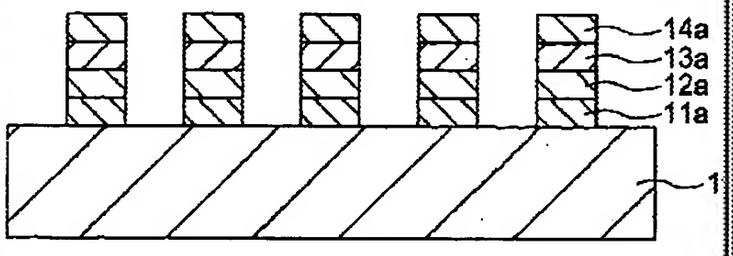


FIG. 7A

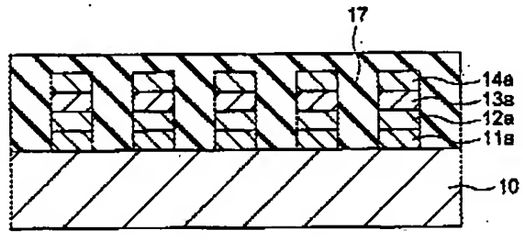


FIG. 7B

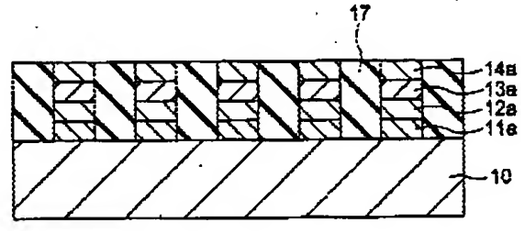
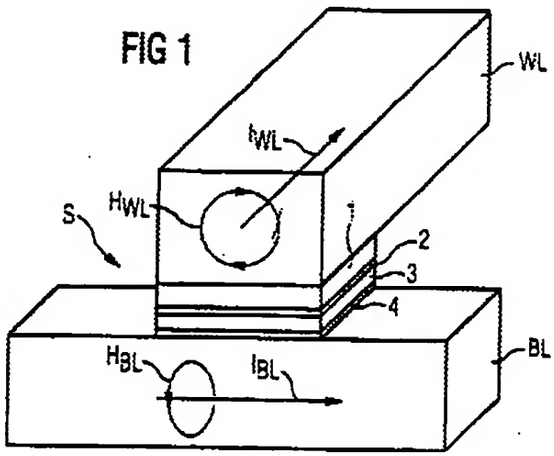


FIG 1



US006351408B1

(12) **United States Patent**
Schwarzl et al.

(10) **Patent No.: US 6,351,408 B1**
(45) **Date of Patent: Feb. 26, 2002**

(54) **MEMORY CELL CONFIGURATION**

(75) Inventors: Siegfried Schwarzl; Lothar Risch, both of Neubiberg (DE)

(73) Assignee: Infineon Technologies AG, Munich (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No. 09/544,761

(22) Filed: Apr. 6, 2000

Related U.S. Application Data

(63) Continuation of application No. PCT/DE98/02875, filed on Sep. 28, 1998.

(30) **Foreign Application Priority Data**

Oct. 6, 1997 (DE) 197 44 095

(51) Int. Cl.[7] G11C 11/00

(52) U.S. Cl. 365/158; 365/171; 365/209; 365/207; 365/173; 365/145

(58) Field of Search 365/158, 171, 365/209, 207, 173, 145

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"Spin-Valve RAM Cell" (Tang et al.), dated Nov. 1995, IEEE Transactions on Magnetics, vol. 31, No. 6, pp. 3206-3208, as mentioned on p. 3 of the specification.
"An IC process compatible Nonvolatile Magnetic RAM" (Tang et al.), IEDM 95—697, pp. 5.7.1 to 5.7.3.

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Primary Examiner—Richard Elms
Assistant Examiner—Vanthu Nguyen
(74) *Attorney, Agent, or Firm*—Herbert L. Lerner; Laurence A. Greenberg; Werner H. Stemer

(57) **ABSTRACT**

A memory cell configuration has word lines and bit lines running transversely with respect thereto. Memory elements with a magnetoresistive effect are respectively connected between one of the word lines and one of the bit lines. The memory elements are disposed in at least two layers one above the other.

9 Claims, 3 Drawing Sheets

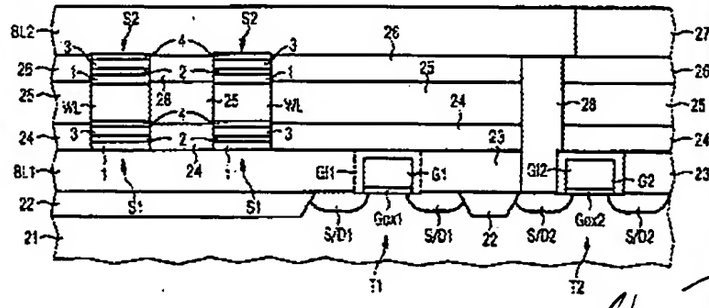

Fig 2

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